WHAT IS CLAIMED IS

1. A flyback power converter comprising:

a transformer having a secondary winding, a first primary winding, and a second primary winding, wherein said first primary winding has a first terminal and a second terminal, said second primary winding has a first terminal and a second terminal, wherein said second terminal of said first primary winding is connected to said first terminal of said second primary winding, and said second terminal of said second primary winding is connected to a ground reference;

an output rectifier connected from said secondary winding to an output of the power converter;

a switching transistor for controlling the voltage across the primary windings of the transformer, wherein a drain of said switching transistor is connected to an input of the power converter;

a current-sense resistor for generating a current-sense voltage, wherein said current-sense resistor is connected between a source of said switching transistor and said first terminal of said first primary winding;

a PWM controller for regulating a switching frequency and for providing a PWM signal to drive a gate of said switching transistor, wherein said PWM controller has a supply-voltage input for receiving power, a detection input for receiving a flyback voltage, a current-sense input for current detection, a compensation input for frequency compensation, and a ground-reference input connected to said first terminal of said first primary winding, and wherein said current-sense input is connected to said source of said switching transistor;

a power-pin capacitor for starting up said PWM controller, wherein said power-pin capacitor is connected between said supply-voltage input of said PWM controller and said ground-reference input of said PWM controller;

a start-up resistor for charging said power-pin capacitor, wherein said start-up resistor is connected from said input of the power converter to said supply-voltage input of said PWM controller;

a power-pin diode connected from said second terminal of said first primary winding to said supply-voltage input of said PWM controller;

a detection resistor for receiving an offset current to compensate for the voltage drop across said output rectifier, wherein said detection resistor is connected from said second terminal of said first primary winding to said detection input of said PWM controller;

a compensation capacitor connected from said compensation input of said PWM controller to said ground-reference input of said PWM controller;

a transient voltage suppressor connected in parallel with said second primary winding; and

a snubber diode connected in series with said transient voltage suppressor.

2. The flyback power converter as claimed in claim 1, wherein the output current of the power supply and the output voltage of the power supply are regulated in a substantially constant manner.

3. The flyback power converter as claimed in claim 1, wherein said flyback voltage is reflected from said secondary winding to said first primary winding and said second primary winding of said transformer, wherein said flyback voltage is reflected in response to the falling edge of said PWM signal.

4. The flyback power converter as claimed in claim 1, wherein a sampled voltage is

sampled from said flyback voltage through said detection input of said PWM controller, and said flyback voltage is sampled after the falling-edge of said PWM signal and is sampled before the transformer current drops to zero.

5. The flyback power converter as claimed in claim 1, wherein a primary current of said transformer is produced during the on-time of said PWM signal, and said primary current of said transformer generates a current-sense voltage across said current-sense resistor.

6. The flyback power converter as claimed in claim 1, wherein said offset current is pulled from said detection input of said PWM controller, and said offset current is modulated so that the amplitude is inversely proportional to the operating temperature of the flyback power converter.

7. The flyback power converter as claimed in claim 1, wherein said PWM signal is modulated in a manner that the DC output voltage is kept substantially constant in response to said sampled voltage.

8. The flyback power converter as claimed in claim 1, wherein said switching frequency is controlled in response to a clamped-sample voltage of the PWM controller and is controlled in a manner that keeps the output current of the flyback power converter substantially constant.

9. The flyback power converter as claimed in claim 1, wherein said PWM controller comprises:

a double sample amplifier for sampling said flyback voltage from said detection input of said PWM controller, wherein said double sample amplifier produces said clamped-sample voltage, said sampled voltage obtained from said detection input of said PWM controller, and a feedback voltage obtained by amplifying said sampled voltage;

an oscillator for regulating said switching frequency and for producing a clock signal in response to said clamped-sample voltage, wherein said clamped-sample voltage is obtained by clamping said sampled voltage;

a PWM circuit for generating said PWM signal, wherein said PWM signal is a function of said feedback voltage, said current-sense voltage, and a limit voltage;

a pulse generator for generating sampling pulses in response to said PWM signal and said clock signal, wherein said flyback voltage is sampled in response to said sampling pulses;

a hysteresis comparator for measuring the current flow through said transformer; and

a threshold voltage source connected to said hysteresis comparator.

10. The PWM controller as claimed in claim 9, wherein said double sample amplifier comprises:

a first switch and a second switch having input terminals connected to said detection input of said PWM controller, wherein said first switch and said second switch are respectively turned on/off by a first sampling pulse and a second sampling pulse;

a first capacitor and a second capacitor connected to an output terminal of said first switch and an output of said second switch respectively, wherein said first capacitor produces a first hold voltage and said second capacitor produces a second hold voltage;

a discharge switch connected from said second capacitor to the ground reference, wherein said discharge switch is turned on/off by said PWM signal;

a signal buffer consisting of a first operational amplifier, a second operational amplifier, said first capacitor, said second capacitor, a first diode, and a second diode, wherein said first operational amplifier and said second operational amplifier respectively have positive input terminals connected to said second capacitor and said

first capacitor, wherein an output of said signal buffer further connects to a negative input terminal of said first operational amplifier and a negative input terminal of said second operational amplifier, and wherein said first diode and said second diode are respectively connected from output terminals of said first operational amplifier and said second operational amplifier to said output of said signal buffer;

a third switch having an input terminal connected to said output of said signal buffer, wherein said third switch is turned on/off by a third sampling pulse;

a third capacitor for producing said sampled voltage, wherein said third capacitor is connected to an output terminal of said third switch;

a third operational amplifier having a positive input terminal connected to said third capacitor;

a clamp resistor connecting to an output of said third operational amplifier, wherein said third operational amplifier outputs said clamped-sample voltage via said clamp resistor, wherein a negative input terminal of said third operational amplifier is coupled to said clamp resistor;

a clamp current source for ensuring that said clamped sample voltage exceeds a minimum voltage level, wherein said clamp current source is connected to said clamp resistor;

a first DSA transistor;

a fourth operational amplifier having an output terminal for driving a gate of said first DSA transistor, wherein a negative input terminal of said fourth operational amplifier is connected to a source of said first DSA transistor;

a gain resistor coupled to said negative input terminal of said fourth operational amplifier and said source of said first DSA transistor;

a DSA reference voltage source for providing a reference voltage for said double sample amplifier, wherein said DSA reference voltage source is connected to a positive input terminal of said fourth operational amplifier;

a first current mirror consisting of a first input transistor and a first output transistor, wherein a drain of said first input transistor is connected to a drain of said first DSA transistor;

a DSA output resistor for generating said feedback voltage, wherein said DSA output resistor is connected to a drain of said first output transistor;

a reference current source;

a programmable current generator connected to said reference current source, wherein said programmable current generator produces a programmable current, and the amplitude of said programmable current is modulated to be inversely proportional to the operating temperature of the flyback power converter.

an offset current mirror having an input terminal connected to a joint of said programmable current generator and said reference current source, wherein an output terminal of said offset current mirror is connected to said detection input of said PWM controller, and said output terminal of said offset mirror current pulls said offset current; and

a DSA-input diode connected from said detection input of said PWM controller to the ground reference;

11. The double sample amplifier as claimed in claim **10**, wherein the magnitude of the output voltage of said double sample amplifier is equal to the magnitude of the maximum of said first hold voltage and said second hold voltage.

12. The double sample amplifier as claimed in claim **10**, wherein said programmable

current generator comprises:

a second current mirror consisting of a second input transistor, a second left-output transistor and a second right-output transistor, wherein the supply voltage is supplied to said second current mirror;

a bipolar current mirror consisting of an input bipolar transistor and an output bipolar transistor; wherein a collector of said input bipolar transistor is connected to a drain of said second left-output transistor, and a collector of said output bipolar transistor is connected to a drain of said second input transistor;

a first resistor connected between an emitter of said output bipolar transistor and the ground reference; and

a third current mirror consisting of a third input transistor and a third output transistor, wherein a drain of said third output transistor pulls said programmable current.

13. The PWM controller as claimed in claim 9, wherein said oscillator comprises:

a variable current generator for receiving said clamped-sample voltage, wherein said variable current generator comprises an error amplifier, a V-to-I transistor, and a second resistor;

a fourth current mirror for generating a fourth mirror current and an OSC charge current, wherein said fourth current mirror comprises a fourth input transistor, a fourth left-output transistor and a fourth right-output transistor;

a fifth current mirror consisting of a fifth input transistor and a fifth output transistor, wherein a drain of said fifth input transistor receives said fourth mirror current and pulls an OSC discharge current;

an first inverter;

an OSC capacitor;

a first comparator and a second comparator, wherein a second reference voltage is supplied to a positive input terminal of said first comparator, and a first reference voltage is supplied to a negative input terminal of said second comparator;

an OSC current source;

a fourth switch for conducting the OSC charge current, wherein said fourth switch is controlled by an output of said first inverter;

a fifth switch for conducting said OSC discharge current; and

a first NAND-gate and a second NAND-gate, wherein said first NAND-gate produces said clock signal controlling said fifth switch and drives an input of said first inverter.

14. The PWM controller as claimed in claim **9**, wherein said PWM circuit comprises:

a second inverter;

a third comparator for comparing said feedback voltage with the current-sense voltage;

a fourth comparator for comparing said limit voltage with said current-sense voltage;

a third NAND-gate having a first input terminal connected to an output terminal of said third comparator, wherein said third NAND-gate has a second input terminal connected to an output of said fourth comparator;

a fourth NAND-gate having a first input terminal, wherein a first input terminal of said fourth NAND-gate is driven by an output of said third NAND-gate;

a first AND-gate for supplying said PWM signal;

a first flip-flop having a clock input driven by an output of said second inverter; and

a blanking circuit having an input terminal driven by said PWM signal, wherein said blanking circuit has an output terminal connected to a second input terminal of said fourth NAND-gate.

15. The PWM circuit as claimed in claim **14**, wherein said blanking circuit comprises:

a means for producing a blanking time comprising a BLK transistor, a BLK current source, a BLK capacitor, and a BLK inverter;

a BLK input inverter for supplying said PWM signal to a gate of said BLK transistor, wherein said PWM signal is supplied to an input of said BLK input inverter, said input of said BLK input inverter is an input terminal of said blanking circuit, and said blanking time starts substantially soon following each rising-edge of the PWM signal; and

a BLK NAND-gate for supplying a blank signal, wherein said PWM signal is supplied to a first input of said BLK NAND-gate, and said BLK NAND-gate has a second input connected to an output of said BLK inverter.

16. The PWM controller as claimed in claim **9**, wherein said pulse generator comprises:

a means for producing a sampling clock signal comprising a first PG current source, a first PG switch, a second PG current source, a first PG capacitor, a PG hysteresis buffer and a first PG inverter, wherein said first PG current source and said second PG current source respectively determine an on-time and an off-time of said sampling clock signal;

a means for producing a delay time comprising a second PG inverter, a third PG inverter, a first PG transistor, a third PG current source and a second PG capacitor;

a second AND-gate for generating a first sampling pulse;

a third AND-gate for generating a second sampling pulse;

a second flip-flop for enabling/disabling said second AND-gate and said third AND-gate;

a third flip-flop;

a fourth PG inverter;

an OR-gate having a first input for receiving an inverse output of said third flip-flop and a second input for receiving an output of said hysteresis comparator;

a fourth AND-gate having a first input terminal for receiving said sampling clock signal, a second input terminal coupled to said second PG capacitor, and a third input terminal connected to an output of said second PG inverter; and

a means for producing said third sampling pulse comprising a fifth PG inverter, a second PG transistor, a fourth PG current source, a third PG capacitor, a sixth PG inverter, and a fifth AND-gate.